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Design of Optical Pulse Position Modulation (PPM) Translating Receiver

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Introduction

M-ary pulse position modulation (*M*-ary PPM) signaling is a means of transmitting multiple bits per symbol in an intensity modulated/direct detection (IM/DD) system [1]. PPM is used in applications with average power limitations. In optical communication systems, PPM becomes challenging to implement at gigabit rates and/or large *M*, since pulsed signaling requires higher electronic processing bandwidths than the fundamental transmission rate. We have thus been exploring techniques for PPM communications using optical processing. Previous work described a transmitter algorithm that directly translates a bit sequence of *N* digital bits to the optical pulse position *m* for any $M=2^N$ [2]. It has been considerably more difficult to define a similar receiver algorithm that translates the received optical pulse position directly back to a bit sequence with minimal electronic processing. Designs for specific *M*s (e.g., 4-ary) have been shown and implemented [3], but are difficult to scale to larger *M* [2,4]. In this work, we present for the first time a generalized PPM translating receiver that is applicable to all *M* and data rates.

PPM Translating Receiver Algorithm Description

The receiver algorithm we propose utilizes the fact that a PPM symbol, *m*, uniquely represents one of $M = 2^N$ values within the set $S = \{0,1,2,\ldots,m,\ldots,M-2,M-1\}$. *m* can be represented in binary format as

$$m = b_{N-1}2^{N-1} + b_{N-2}2^{N-2} + \ldots + b_n 2^n + b_2 2^2 + b_1 2^1 + b_0 2^0$$
$$= \sum_{n=0}^{N-1} b_n 2^n$$

where b_n is the binary value (0 or 1) of the corresponding bit within the sequence of *N* bits. The PPM symbol is transmitted as a pulse contained within a PPM frame. The frame has *M* slots and the pulse, of width < T_s, is transmitted at the *m*th slot (synchronization assumed).

As with all PPM schemes, the proposed receiver performs a comparison test among the *M* slots in a frame and determine which slot contains the pulse representing the symbol *m*. An example implementation is shown in Fig. 1 for the case of $M = 16$. This can be done optically by making multiple copies of the incoming frame using a coupler and aligning each frame incrementally from 0 to *M*-1 slot positions using optical delays. This allows all slots to be aligned on a parallel bus for comparison, and the output of each bus is designated as a slot line (s*m* in Fig. 1). Once each slot is aligned and separated onto separate slot lines, copies of each slot are combined into *N* separate photodetectors corresponding to each bit of the transmitted symbol. Depending on the binary value, the slot line copy is then made to be either positive (representing 1) or negative (representing 0). Copying and combining the slots can again be implemented with optical couplers. The bipolar slot value is produced by selectively sending the slot copies to the positive or negative terminals of a balanced photodetector. The key to generalizing this algorithm for all *M* is determining which slot copies should be sent to the positive or negative terminals of the balanced photodetector. Given that a photodetector produces the *n*th bit of transmitted symbol *m*, the assignment of the *m*th slot line to the positive or negative terminal of this photodetector is determined by calculating $m/2^n$. If the quotient (ignore the remainder) is an odd value, then the slot line is forwarded to the positive terminal of the photodetector. If the quotient is even, it is forwarded to the negative terminal. At this point, one can place optical gates prior to each photodetector terminal to simultaneously sample all slots. As multiple copies of the original frame have been made, this eliminates all copies of the original pulse except for the ones that are properly aligned to the correct slot. The resulting outputs can then be optical-to-electrically converted by photodetectors whose bandwidths only need to operate at the frame rate, rather than the slot rate. (Note that optical gating can be replaced by electrical sampling in slower systems.) Optimized implementation of the algorithm requires using an erbium-doped waveguide amplified ("lossless") planar lightwave circuit (EDWA/PLC), which will provide the precision required to set the delays of the slots while minimizing the insertion losses that are inherent in the algorithm. Fig. 1 does not show the optical gates, which would be placed at the input to the differential receivers.

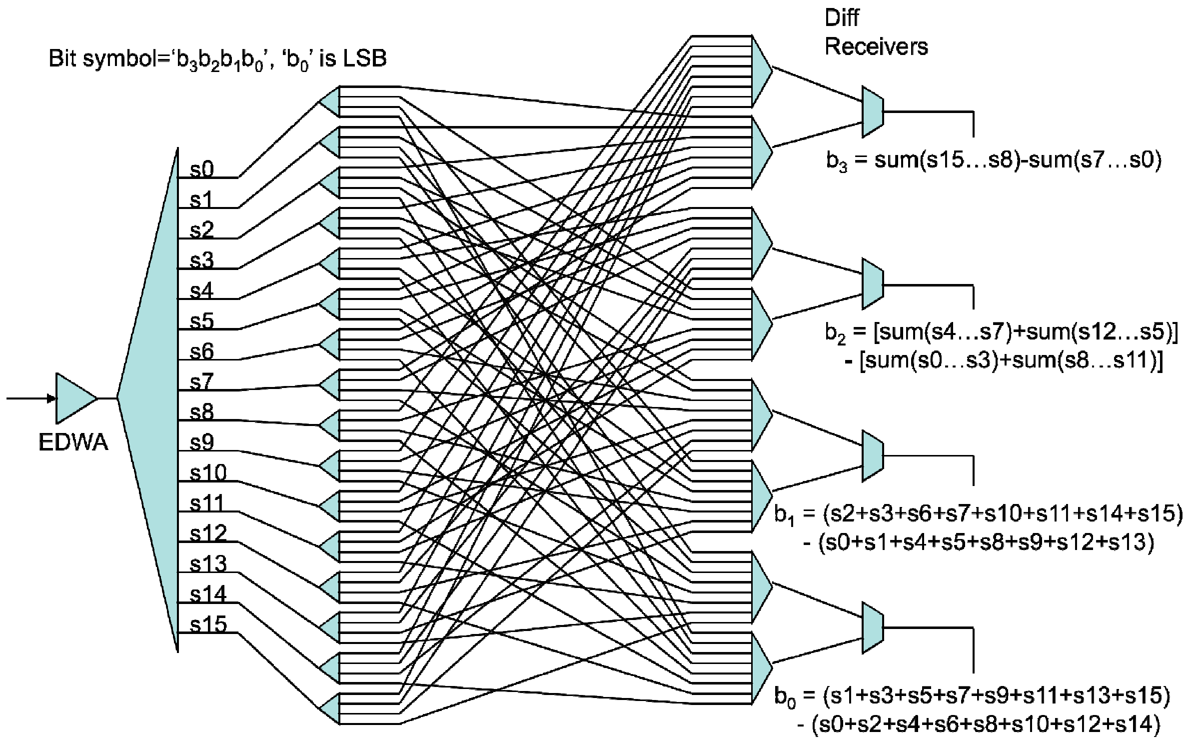

Figure 1. Design of the *16-ary* PPM Receiver That Directly Translates Pulse-Position to Bit Sequence at the Frame Rate.

Summary and Conclusions

We have described a design for a receiver that directly converts PPM pulse positions into bit sequences for arbitrary *M* and data rate. The design is enabled by lossless splitters based on EDWA/PLCs.

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Abstract
Translating the received PPM symbol stream to its originating bit sequence is challenging at large M and/or high data rates. We describe a frame rate translating algorithm and associated receiver design enabled by lossless splitters.

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